Remarks

The Examiner has rejected claims 1-5, 7-10, 12-14 and 22 as being unpatentable over the combination of Roland, et al '723 in view of Dufour '835 and Faris '671. Claims 15-19 have been rejected as unpatentable over the combination of Roland, et al '723 in view of Hastings, et al '196 and Faris '671. Claim 21 has been rejected as being unpatentable over Roland, et al '723 in view of Faris '671. Claim 20 has been rejected as being anticipated by Roland, et al '723. Claims 6 and 11 have been objected to as being dependent upon a rejected-base claim but have been found to otherwise be of allowable scope.

Responsive to the foregoing, applicants have amended independent claim 20 to include the limitations of allowable claim 6; as the Examiner has acknowledged that the art does not teach or suggest an attenuator in which a resistive layer comprises two conductive strips and trapezoidal regions as recited in claim 6, it is believed that claim 20 is of allowable scope. New independent claim 23 incorporates the features of claim 11 and its base claim 1. Claim 6 has been canceled.

With respect to the rejections, applicants respectfully traverse the rejections as follows:

The present invention is directed to a microwave dissipater/attenuator device in which a resistive layer is formed on an insulating substrate. Independent claims 1, 15, 21, and 22 of the present application each recites, inter alia, that the resistive layer is covered at least in part by a ground plane connected to a ground zone and insulated from the resistive layer by an insulating layer.

The primary Roland, et al. '723 reference discloses a microwave circuit attenuator having an input conductor (40) connected through a first resistive element (44) to a first grounding connector (50). As acknowledged by the Examiner, Roland, et al. '723 neither discloses nor suggests that the resistive layer is to be covered by a ground plane insulated from the resistive layer by an insulating layer. Such a feature is further not disclosed or properly suggested by Faris '671 or Dufour '835.

Faris '671 is directed to a method of fabricating vertical integrated circuits. That is, a semiconductor device in which microdevices are stacked in a vertical integration. Faris '671 teaches the use of edge interconnects between the layers instead of through interconnects. Column 30, lines 22-24. When such edge interconnects are used, Faris '671 teaches that shielding layers may be provided between adjacent circuit layers to prevent cross noise between the circuit elements on the different layers. The shielding layer prohibits noise created by one layer to be transmitted to an adjacent layer. Faris '671 further teaches that such shielding is particularly desirable for mixed, vertically-integrated circuits having combinations of power, analog, RF, digital, optical, photonic, MEM and microfluidic devices. Faris '671 offers no suggestion that its shielding is to serve as a microwave groundplane Further, Roland, et al. '723 is not related to vertical integrated circuit technology, and one skilled in the art would not reasonably look to the teachings of Faris '671 and its stated vertical integrated circuit technology for guidance as to how to improve a ground plane configuration in a microwave attenuator. It is only with the hindsight developed by the present invention that one can in any way associate the teachings of Roland, et al '723 and Faris '671 as offered by the Examiner, and the use of such hindsight is not a valid basis for claim rejection.

Dufour '835 discloses the production of conductive layers on an insulating substrate by use of a silk screen-printing process. Such teaching fails to cure the deficiency of the combination of Roland, et al. '723 and Faris '671, as it provides absolutely no suggestion of an at least partially covering ground plane over a resistive layer for dissipating and/or attenuating power.

As each of the rejected claims of the present application includes the feature of an at least partially covering ground plane, and neither Roland, et al. '723 itself, or in combination with Faris '671 and any other art of record, teach or suggest such a construction, it is respectfully submitted that none of the claims of the present application are rendered unpatentable or anticipated by the art of record and, accordingly, all claims are allowable.

Withdrawal of the rejections and passage to allowance is solicited.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the U.S. Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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